

**CLAIMS**

We claim:

1. A method for designing an integrated circuit comprising:
  - partitioning a design into a plurality of function blocks;
  - designing a first one of said plurality of function blocks employing Verilog to produce a first block design;
  - 5       designing a second one of said plurality of function blocks employing SPICE to produce a second block design;
  - converting said first block design to SPICE to produce a converted first block design;
  - simulating operation of said converted first block design and said second block design; and
  - 10       translating said converted first block design to Verilog to produce a translated first block design.
2. The method of claim 1 further comprising:
  - comparing said translated first block design with said first block design.
3. The method of claim 1 wherein said step of translating further comprises:
  - changing ".SUBCKT" instances to "module".
4. The method of claim 1 wherein said step of translating further comprises:
  - changing ".ENDS" statements to "endmodule".
5. The method of claim 1 wherein said step of translating further comprises:
  - deleting a discrete circuit element description.
6. The method of claim 1 wherein said step of translating further comprises:
  - defining a wire name corresponding to a SPICE node name.

7. The method of claim 1 wherein said step of translating further comprises:  
identifying a SPICE output signal name and defining a Verilog output  
signal using said output signal name.
8. The method of claim 1 wherein said step of translating further comprises:  
identifying a SUBCKT name;
9. The method of claim 8 wherein said step of translating further comprises:  
employing said SUBCKT name as a module name;
10. A method for translating a SPICE netlist to Verilog comprising:  
opening a SPICE file;  
translating ".SUBCKT" instantiations to "module";  
translating ".ENDS" statements to "endmodule";  
translating SPICE circuit elements to Verilog format; and  
removing discrete circuit elements.
11. The method of claim 10 further comprising:  
saving the file.
12. The method of claim 10 wherein said step of translating further comprises:  
identifying a SPICE input signal name and defining a Verilog wire  
employing said input signal name.
13. The method of claim 10 wherein said step of translating further comprises:  
identifying an input signal name through a naming convention.
14. The method of claim 10 wherein said step of translating further comprises:  
identifying an input signal name through a predefined delimiter.

15. The method of claim 10 further comprising:

identifying a SUBCKT name.

16. The method of claim 15 wherein said step of translating further comprises:

employing said SUBCKT name as a module name.

17. An integrated circuit produced by the steps of:

partitioning a design into a plurality of function blocks;

designing a first one of said plurality of function blocks employing

Verilog to produce a first block design;

5 designing a second one of said plurality of function blocks employing

SPICE to produce a second block design;

converting said first block design to SPICE to produce a converted first  
block design;

10 simulating operation of said converted first block design and said second  
block design; and

translating said converted first block design to Verilog to produce a  
translated first block design.

18. The integrated circuit of claim 17 further comprising:

comparing said translated first block design with said first block design.

19. The integrated circuit of claim 17 wherein said step of translating further  
comprises:

changing ".SUBCKT" instances to "module".

20. The integrated circuit of claim 17 wherein said step of translating further  
comprises:

changing ".ENDS" statements to "endmodule".

21. The integrated circuit of claim 17 wherein said step of translating further comprises:
  - deleting a discrete circuit element description.
22. The integrated circuit of claim 17 wherein said step of translating further comprises:
  - defining a wire name corresponding to a SPICE node name.
23. The integrated circuit of claim 17 wherein said step of translating further comprises:
  - identifying a SPICE output signal name and defining a Verilog output signal using said output signal name.
24. The integrated circuit of claim 17 wherein said step of translating further comprises:
  - identifying a SUBCKT name.
25. The integrated circuit of claim 24 wherein said step of translating further comprises:
  - employing said SUBCKT name as a module name.